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10/731,950	12/10/2003	Woong-Kwon Kim	10125/4132	6763

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EXAMINER	
NGUYEN, HOAN C	
ART UNIT	PAPER NUMBER
2871	
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12/06/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/731,950	KIM ET AL.	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6-13,18,19,22-35 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-13,18,19,22-35 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to claims 18 and 46 based on the Response filed on 10/20/2010 have been considered but are moot in view of the new ground(s) of rejection. Therefore, this is Final action.

Response to Arguments

Applicant's arguments filed on 10/20/2010 have been fully considered but they are not persuasive.

Applicant's ONLY arguments are follows:

As best understood, Yamamoto et al. will dispose the black matrix made of the black resin, which is indeed a non-transparent layer, between the thin film transistor and the liquid crystal layer. However, claims 1, 18, 35 and 46 recites "the plurality of transparent layers fills a space between the thin film transistor and the liquid crystal layer". Therefore, the teachings of Yamamoto et al. teach away from the claimed invention.

Examiner's responses to Applicants' ONLY arguments are follows:

Yamamoto et al. disclose "the plurality of transparent layers" and the black resin fill a space between the thin film transistor and the liquid crystal layer. The claims 1, 18, 35 and 46 do not cite "ONLY the plurality of transparent layers (color filters)" **without**

the black resin fill a space between the thin film transistor and the liquid crystal layer"; therefore, the argument is irrelevant and Yamamoto et al. DID NOT teach away from the cited claims [attention: examiner would exam ONLY the cited CLAIMS, not the claimed invention in the specification].

However, Figure 5 in the instant application shows "ONLY the plurality of transparent layers fills a space between the thin film transistor and the liquid crystal layer", which is not cited in the claims 1, 18, 35 and 46. Therefore, in order to overcome the Yamamoto et al., the independent claims 1, 18, 35 and 46 should be amended with feature "ONLY the plurality of transparent layers without any black matrix or non-transparent layer fills a space between the thin film transistor and the liquid crystal layer". Then the rejections in the last non-final action have been repeated below:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The secondary reference Midorikawa et al. (US 6281955 B1) *disclose the plurality of pixel electrodes 30 formed directly on top surfaces of the plurality of color filters 24;* ***Midorikawa et al. fail to*** *disclose "the first and second top surfaces face the common electrode and have the*

same level". However, the primary reference Yamamoto et al. (US6445432B2) discloses "the first and second top surfaces face the common electrode and have the same level".

1. Claims 1, 6-12, 18, 22-31, 35 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of **Midorikawa et al. (US 6281955 B1)**.

Yamamoto et al. teach (Figs. 2-4) a liquid crystal display device comprising:

Claims 1, 18, 35 and 46:

- a plurality of gate lines 3a formed on a first substrate along a transverse direction, each gate line including a gate electrode 3;
- a first insulating layer (gate insulating layer 4) formed on the first substrate to cover the gate lines and the gate electrodes;
- a plurality of data lines 6a formed on the first insulating layer along a longitudinal direction, the data lines defining a plurality of pixel regions with the gate lines and each including a source electrode 6;
- a thin film transistor formed at a crossing region of each of the gate and data lines, each thin film transistor including one of the gate electrodes, a semiconductor layer 5, one of the source electrodes, and a drain electrode;
- a color filter R over the first insulating layer in each pixel region, each color filter having one of red, green and blue colors R/G/B, the color filters having a plurality of drain contact holes exposing the drain electrodes 7; each color filter having a first top surface;

- a pixel electrode 15 over a the first top surface in each pixel region, each pixel electrode contacting one of the drain electrodes through the drain contact hole, wherein a portion of the pixel electrode in the drain contact hole contacts inner side surfaces of the color filter defining the drain contact hole (see Figure 2 below);
- a common electrode on a second substrate 16, the common electrode facing the first substrate; and
- a liquid crystal layer 20 interposed between the common electrode and the pixel electrodes.
- plurality of transparent layers (color filters) including light shielding color filter patterns and the black resin filling a space between the thin film transistor and the liquid crystal layer 20, the light shield color filter color patterns including at least two of red, green or blue resins, the light-shielding color filter patterns having a second top surface,

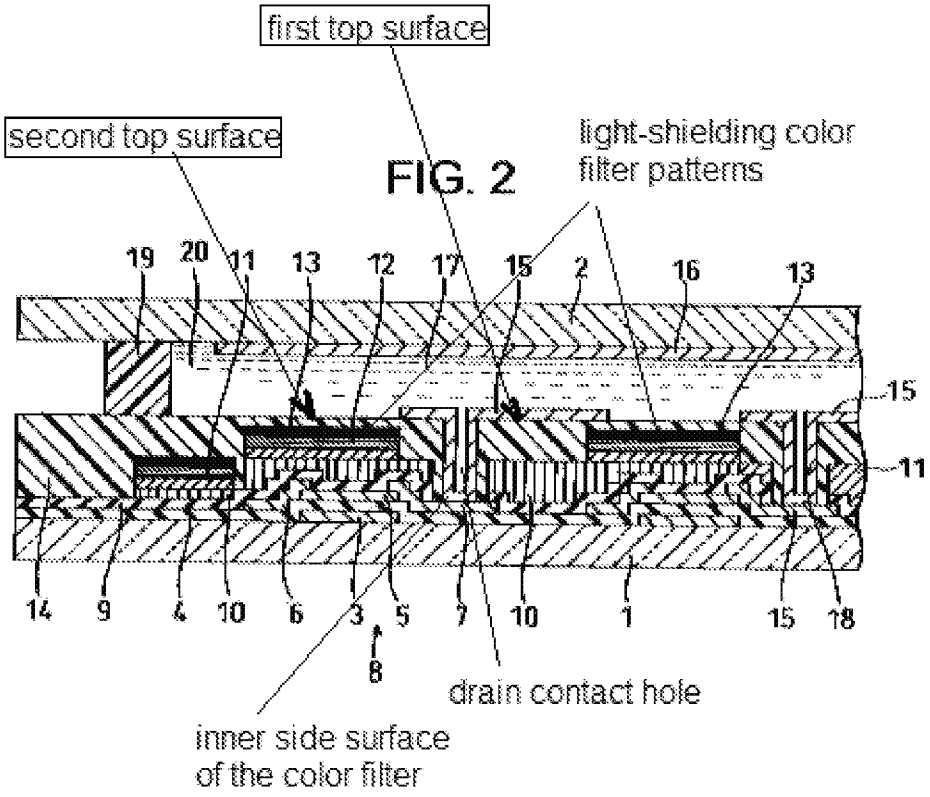


FIG. 2

wherein

- a thickness of the light-shielding color filter patterns is equal to or less than a thickness of the color filter,
- the first and second top surfaces face the common electrode and have the same level of the surface of the flattening film 14.

Claims 1 and 22:

- the light-shielding color filter patterns are formed of the same material as the color filters.

Claims 6 and 23:

- a cell gap between the light-shielding color filter patterns and the common electrode is greater than zero.

Claims 7 and 24:

- the color filters are formed of a photosensitive resin through a photolithography process.

Claims 8 and 25:

- red, green and blue color filters are formed sequentially from the semiconductor layers towards the liquid crystal layer.

Claims 9 and 26:

- each of red, green and blue color filter patterns (at shielding regions) has a thickness smaller than each of red, green and blue color filters (at display regions).

Claims 10 and 27:

- each light-shielding color filter pattern has a red color filter pattern, a green color filter pattern and a blue color filter pattern.

Claims 11 and 28-29:

- a second insulating layer 9 between the thin film transistors 5 and the light-shielding patterns and between the first insulating layer 4 and the color filters, wherein the second insulating layer 9 covers the source electrodes 6, the drain electrodes 7 and the data lines and wherein the drain contact holes extend through the second insulating layer 9 wherein performing etching (Fig. 3C) an exposed portion of the second insulating layer such that the drain contact holes extend through the second insulating layer to expose a portion of each drain electrode.

Claims 12 and 30-31:

- a third insulating layer (a flattened film 14) between the color filters and the pixel electrodes, wherein the third insulating layer 14 covers the color filters and the light-shielding color filter patterns, wherein performing etching a portion of the third insulating layer corresponding to the drain contact holes such that the drain contact holes extend through the third insulating layer to expose a portion of each drain electrode.

However, Yamamoto et al. fail to disclose the plurality of pixel electrodes are formed directly on top surfaces of the plurality of color filters.

Midorikawa et al. (US 6281955 B1) teach (Fig. 1) the plurality of pixel electrodes 30 formed directly on top surfaces of the plurality of color filters 24 for obtaining high quality color images due to reducing the electrical coupling between color filter and TFT (col. 2 lines 45-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with the plurality of pixel electrodes formed directly on top surfaces of the plurality of color filters for obtaining high quality color images due to reducing the electrical coupling between color filter and TFT (col. 2 lines 45-48).

In the following 103-rejection, both primary reference Yamamoto et al. (US6445432B2) and secondary reference ***Yanai (US 6137552 A)*** *disclose "the first and second top surfaces face the common electrode and have the same level".*

2. Claims 1, 6-12, 18, 22-31, 35 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of **Yanai (US 6137552 A).**

Yamamoto et al. teach (Figs. 2-4) a liquid crystal display device comprising:

Claims 1, 18, 35 and 46:

- a plurality of gate lines 3a formed on a first substrate along a transverse direction, each gate line including a gate electrode 3;
- a first insulating layer (gate insulating layer 4) formed on the first substrate to cover the gate lines and the gate electrodes;
- a plurality of data lines 6a formed on the first insulating layer along a longitudinal direction, the data lines defining a plurality of pixel regions with the gate lines and each including a source electrode 6;
- a thin film transistor formed at a crossing region of each of the gate and data lines, each thin film transistor including one of the gate electrodes, a semiconductor layer 5, one of the source electrodes, and a drain electrode;
- a color filter R over the first insulating layer in each pixel region, each color filter having one of red, green and blue colors R/G/B, the color filters having a plurality of drain contact holes exposing the drain electrodes 7; each color filter having a first top surface;
- a pixel electrode 15 over a the first top surface in each pixel region, each pixel electrode contacting one of the drain electrodes through the drain contact hole,

wherein a portion of the pixel electrode in the drain contact hole contacts inner side surfaces of the color filter defining the drain contact hole (see Figure 2 below);

- a common electrode on a second substrate 16, the common electrode facing the first substrate; and
- a liquid crystal layer 20 interposed between the common electrode and the pixel electrodes.
- plurality of transparent layers (color filters) including light shielding color filter patterns and the black resin filling a space between the thin film transistor and the liquid crystal layer 20, the light shield color filter color patterns including at least two of red, green or blue resins, the light-shielding color filter patterns having a second top surface,

wherein

- a thickness of the light-shielding color filter patterns is equal to or less than a thickness of the color filter,
- the first and second top surfaces face the common electrode and have the same level of the surface of the flattening film 14.

Claims 1 and 22:

- the light-shielding color filter patterns are formed of the same material as the color filters.

Claims 6 and 23:

- a cell gap between the light-shielding color filter patterns and the common electrode is greater than zero.

Claims 7 and 24:

- the color filters are formed of a photosensitive resin through a photolithography process.

Claims 8 and 25:

- red, green and blue color filters are formed sequentially from the semiconductor layers towards the liquid crystal layer.

Claims 9 and 26:

- each of red, green and blue color filter patterns (at shielding regions) has a thickness smaller than each of red, green and blue color filters (at display regions).

Claims 10 and 27:

- each light-shielding color filter pattern has a red color filter pattern, a green color filter pattern and a blue color filter pattern.

Claims 11 and 28-29:

- a second insulating layer 9 between the thin film transistors 5 and the light-shielding patterns and between the first insulating layer 4 and the color filters, wherein the second insulating layer 9 covers the source electrodes 6, the drain electrodes 7 and the data lines and wherein the drain contact holes extend through the second insulating layer 9 wherein performing etching (Fig. 3C) an exposed portion of the second insulating layer such that the drain contact holes

extend through the second insulating layer to expose a portion of each drain electrode.

Claims 12 and 30-31:

- a third insulating layer (a flattened film 14) between the color filters and the pixel electrodes, wherein the third insulating layer 14 covers the color filters and the light-shielding color filter patterns, wherein performing etching a portion of the third insulating layer corresponding to the drain contact holes such that the drain contact holes extend through the third insulating layer to expose a portion of each drain electrode.

However, Yamamoto et al. fail to disclose the plurality of pixel electrodes are formed directly on top surfaces of the plurality of color filters.

Yanai teach (Figs 3-4) the plurality of pixel electrodes 13 formed directly on top surfaces of the plurality of color filters 10 [wherein the first and second top surfaces face the common electrode and have the same level].

FIG. 3

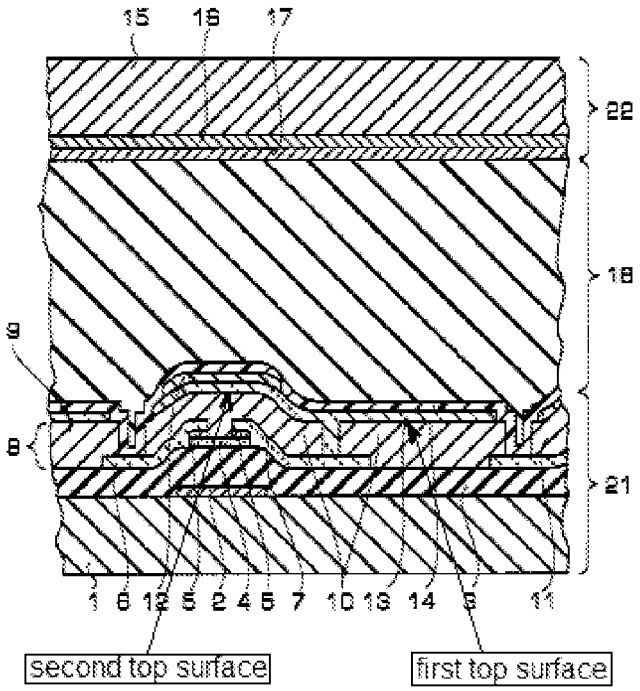
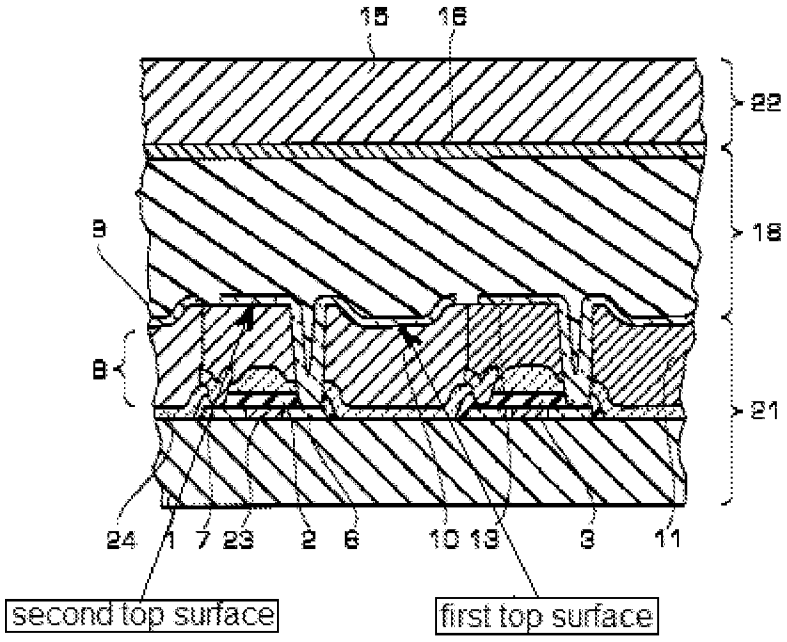


FIG. 4
PRIOR ART



Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with the plurality of pixel electrodes formed directly on top surfaces of the plurality of color filters for improving in its brightness by increasing its aperture ratio while preventing a malfunction of TFTs due to incidence of rays from an external light on a back channel of the TFTs (abstract).

3. Claims 2 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of **Midorikawa et al. (US 6281955 B1)** [or **Yanai (US 6137552 A)]** as applied to claims 1, 6-12, 18, 22-31 and 35 and in further view of Shin (US5825449A).

Yamamoto et al. fail to disclose a liquid crystal display device comprising the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer between the source and drain electrodes as cited in claims 2 and 19.

Shin teaches (Figs. 2-3) a liquid crystal display device comprising the source and drain electrodes are formed on the ohmic contact layer 5 and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer 4 between the source and drain electrodes for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

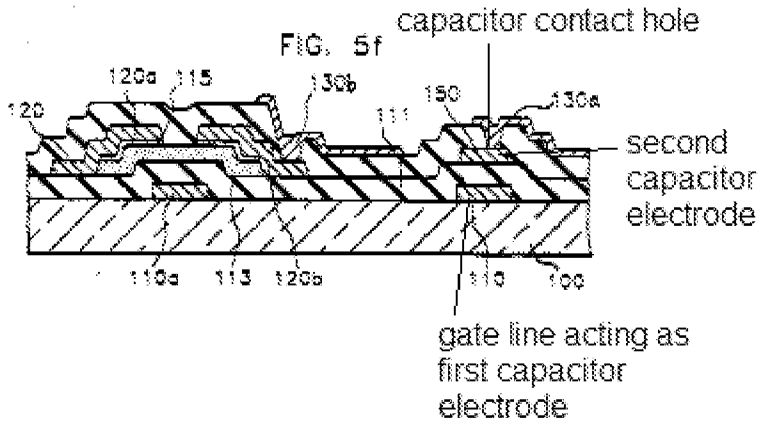
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with the source and drain electrodes are formed on the ohmic contact layer and spaced apart from each other, and wherein each thin film transistor includes a channel on the active layer between the source and drain electrodes for reducing the contact resistance between the active layer and the source/drain regions in the completed device as taught by Shin (col. 1 lines 43-48).

4. Claims 13 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US6445432B2) in view of **Midorikawa et al. (US 6281955 B1)** [or **Yanai (US 6137552 A)]** as applied to claims 1, 6-12, 18, 22-31 and 35 and in further view of Song (US6307602B1).

Yamamoto et al. further disclose a liquid crystal display device comprising colors filters covering gate lines.

Yamamoto et al. fail to disclose a liquid crystal display device comprising a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode on the first insulating layer over each portion of the gate line, wherein each second capacitor electrode and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode. Each color filter includes a capacitor contact hole exposing one of the second capacitor electrodes and wherein the pixel electrodes contacts the second capacitor electrodes through the capacitor contact holes.

Song teaches (Fig. 4a-5f) a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode 150 on the first insulating layer (gate insulating layer 111) over each portion of the gate line, wherein each second capacitor electrode 150 and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode. The passivation layer 117 includes a capacitor contact hole exposing one of the second capacitor electrodes and wherein the pixel electrodes contacts the second capacitor electrodes through the capacitor contact holes.



Combination of **Yamamoto et al.** and Song (Figs. 4-5 show storage electrodes covering gate lines) is obviously replaced the passivation layer by color filters for each pixel, which should includes capacitor contact hole exposing the second capacitor electrode, wherein the pixel electrode contact the second capacitor electrodes through the capacitor contact holes.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a liquid crystal display device as Yamamoto et al. disclosed with a portion of each gate line acts as a first capacitor electrode and a second capacitor electrode 150 on the first insulating layer (gate insulating layer 111) over each portion of the gate line, wherein each second capacitor electrode 150 and portion of the gate line constitute a storage capacitor with the first insulating layer interposed between the portion of the gate line and the second capacitor electrode The color filter includes a capacitor contact hole exposing one of the second capacitor electrodes and wherein the pixel electrodes contacts the second capacitor electrodes through the capacitor contact holes for high display quality with preventing shorting between pixel electrodes as Song taught (col. 2 lines 25-34).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571)272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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